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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/823,076	04/13/2004	Joung-yeal Kim	5649-1229	3985

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Rohan G. Sabapathypillai
Myers Bigel Sibley & Sajovec
Post Office Box 37428
Raleigh, NC 27627

EXAMINER	
MERANT, GUERRIER	
ART UNIT	PAPER NUMBER
2138	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	12/18/2006	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/823,076	KIM ET AL.	
	Examiner	Art Unit	
	Guerrier Merant	2138	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *04/13/04*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-21* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *13 April 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *20040806*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. This is the initial office action based on the application filed on April 13, 2004. Claims 1-21 are currently pending and have been considered below.

Claim Rejections - 35 USC § 101

2. 35 U.S.C. 101 reads as follows:

> a. Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

3. Claims 1-9 are rejected under 35 U.S.C. 101 because the claimed invention lacks patentable utility. The steps of selecting first data from one of a plurality of memory regions in the memory array for output from the memory device via an input/output pad; and then selecting second data from another of the plurality of memory regions for output from the memory device via the input/output pad , do not provide a concrete, tangible, and useful results.

Claim Rejections - 35 USC § 112

4. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> b. The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

5. Claim 1 is rejected under 35 U.S.C. 112, second paragraph, as being incomplete for omitting essential steps, such omission amounting to a gap between the steps. See MPEP § 2172.01. The preamble recites a method for testing a memory cell array however the steps for performing such testing are missing.

Claim Rejections - 35 USC § 102

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> c. A person shall be entitled to a patent unless –
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

7. Claims 1-20 are rejected under 35 U.S.C. 102(a) as being anticipated by Applicant Admitted Prior Art (herein after AAPA).

8. Claims 1, 2, 10, 11 and 12: **AAPA** discloses a circuit and a method for testing a memory cell array of a semiconductor memory device in a parallel bit test mode, comprising: writing test data to a plurality of memory regions in the memory array and reading the test data from the plurality of memory regions *([0011], lines 1-13);* comparing the test data from the plurality of memory regions to produce comparison data that corresponds to the plurality of memory regions selecting first comparison data corresponding to one of the plurality of memory regions for output from the memory device via an input/output pad; and then selecting second comparison data corresponding to another of the plurality of memory regions for output from the memory device via the input/output pad (*[0011], lines 18-26).*

9. Claims 3, 4, 13 and 14: **AAPA** discloses a circuit and a method as in claims 1 and 11 above, wherein the first and second data are both selected from memory

regions sharing a row select control line or from memory regions sharing a column select control line *([0011], lines 1-4).*

10. Claims 5 and 15: **AAPA** discloses a circuit and a method as in claims 1 and 11 above, further comprising replacing a defective row select control line with a redundant row select control line from a row redundant memory cell array *([0011], lines 16-18).*

11. Claims 6 and 16: **AAPA** discloses a circuit and a method as in claims 1 and 11 above, further comprising replacing a defective column select control line with a redundant column select control line from a column redundant memory cell array *([0011], lines 13-16).*

12. Claims 7 and 19: **AAPA** discloses a circuit and a method as in claims 1 and 11 above, wherein the first data is selected in response to a first control signal, and wherein the second data is selected in response to a second control signal *([0010], lines 6-17).*

13. Claims 9 and 18: **AAPA** discloses a circuit and a method as in claims 1 and 11 above, wherein the memory device operates at a double data rate *([0009]).*

Claim Rejections - 35 USC § 103

14. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

15. Claims 8 and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over **AAPA** and further in view of **Tomishima et al. (US 6,470,467 B2).**

16. Claims 8 and 17: **AAPA** discloses a circuit and a method as in claims 1 and 11 above but fails to disclose that the memory device operates at a single data rate. However, **Tomishima et al.** discloses a synchronous semiconductor memory device capable of performing operation test at high speed while reducing burden on tester wherein an SDRAM memory device is operated at a single data rate *(see SDRAM 100; Fig. 1)*. Therefore at the time of the invention, one of ordinary skill in the art would have found it obvious to incorporate the SDRAM memory device of **Tomishima et al.** with the memory device of **AAPA** in order to increase the speed of the memory device.

17. Claim 21 is rejected under 35 U.S.C. 103(a) as being unpatentable over **AAPA** and further in view of **Kim et al. (US 7,013,413 B1)**.

18. Claim 21: **AAPA** discloses a circuit for testing a memory cell array of a semiconductor memory device in a parallel bit test mode, comprising: a multiplexer configured to write test data to a plurality of memory regions in the memory array *([0011], lines 26-32)*; a comparator circuit configured to read the test data from the plurality of memory regions and produce comparison data that corresponds to the plurality of memory regions *([0013])*. But **AAPA** fails to disclose a selecting circuit configured to select first comparison data corresponding to one of the plurality of memory regions for output from the memory device via an input/output pad, and then select second comparison data corresponding to another of the plurality of memory regions for output from the memory device via the input/output pad. However, **Kim et al.** discloses a method for compressing output data and a packet command driving memory device comprising a memory device *(see fig. 4)* wherein *the read data comparing part 500 comprises a number of comparators 501 508 for receiving 8 bits data RD<0:7> read from the core cell region 100 according to a control signal (S_DATEST) when it is a DA mode test, compressing upper 4-bit data RD<0:3> and a lower 4-bit data RD<4:7> and generating a 1-bit data error<i>, 0<i<7, having information indicating whether a failure exists, multiplexers 509-512 for selecting the 8-bit data RD<0:7> read from the core cell region 100 when it is a normal mode or error <0:7> generated by the comparators 501 508 when it is a DA mode test according to the control signal (S_DATEST) (col. 4, lines 55-67).* Therefore at the time of the invention, one of ordinary skill in the art would have found it obvious to incorporate the selector device (multiplexers 509- 512) disclosed in **Kim et al.** in the memory device of **AAPA** in

order *to compress output data that can reduce test time and determine an exact position where a memory failure occurs and a memory device having a pre-fetched data output structure (col.1, lines 1-13,* **Kim et al**.*).*

Conclusion

19. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure:

a) **Fujioka et al (US 6,731,553)**; " Memory Circuit having compressed testing function."

b) **Ochoa et al. (US 6,665,827)**; "Semiconductor integrated circuit having compression circuitry for compressing test data, and the test system for utilizing the semiconductor integrated circuit."

c) **Wright et al. (US 550,026)**; "High speed test system for a memory device."

d) **Schicht (US 6,163,863)**; "Method and circuit for compressing test data in a memory device."

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Exr. Merant Guerrier whose telephone number is (571)

270-1066. The examiner can normally be reached Monday through Thursday from 10: 30 a.m. to 3:30 p.m.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady, can be reached on (571) 272-3819. Draft or Informal faxes, which will not be entered in the application, may be submitted directly to the examiner at (571) 270-2066.

Merant Guerrier
12/08/06

ALBERT DECADY
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100